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Arulpragasam et al.

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[54] **CACHED MULTIPROCESSOR SYSTEM WITH PIPELINE TIMING**

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[52] **U.S. Cl.** **364/200**; 364/900

[58] **Field of Search** ..... 364/200 MS File

[56] **References Cited**

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[57] **ABSTRACT**

A multiprocessor data processing system, the processors (**30**) and input/output devices (**32**) of which share a common control unit (CCU **10**) that includes a write-through cache memory (**20**), a memory management circuit (**22**) and an address translation circuit (**24**). The data processing system further includes random access memory (**28**) and a secondary storage facility (**40, 42, 68, 70**). The processors (**30**) and the input/output devices (**32**) use the memory management circuit (**22**), the address translation circuit (**24**) and the cache memory (**20**) in an ordered pipelined sequence. When a read command "misses" the cache memory (**20**), the CCU accesses the memory modules (**28**) for allocating its cache memory (**20**) and for returning read data to the processors (**30**) or input/output devices (**32**). The CCU also includes a duplicate tag store (**67**) that maintains a copy of the cache memory address tag store (**20A**) thereby to enable the CCU to update its cache memory when data is written into a memory location that is to be maintained in the cache memory.

13 Claims, 24 Drawing Figures